



# Rate Monotonic Analysis

**Introduction**

**Periodic tasks**

**Extending basic theory**

**Synchronization and priority inversion**

**Aperiodic servers**

***Case study: BSY-1 Trainer***



# BSY-1 Trainer Case Study

**This case study is interesting for several reasons:**

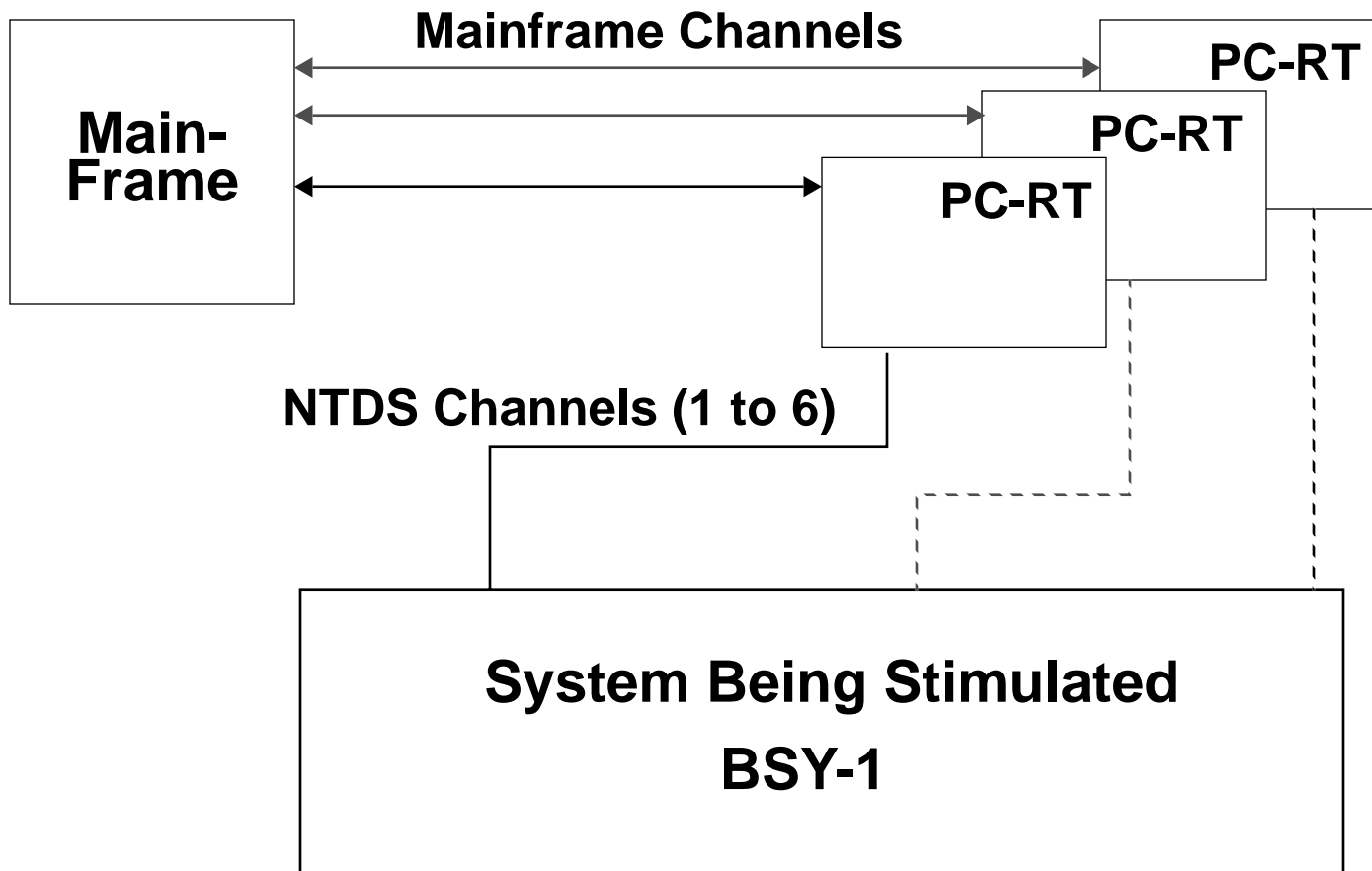
- **RMS is not used, yet the system is analyzable using RMA**
- **“obvious” solutions would not have helped**
- **RMA correctly diagnosed the problem**

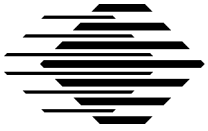
**Insights to be gained:**

- **devastating effects of nonpreemption**
- **how to apply RMA to a round-robin scheduler**
- **contrast conventional wisdom about interrupt handlers with the results of an RMA**

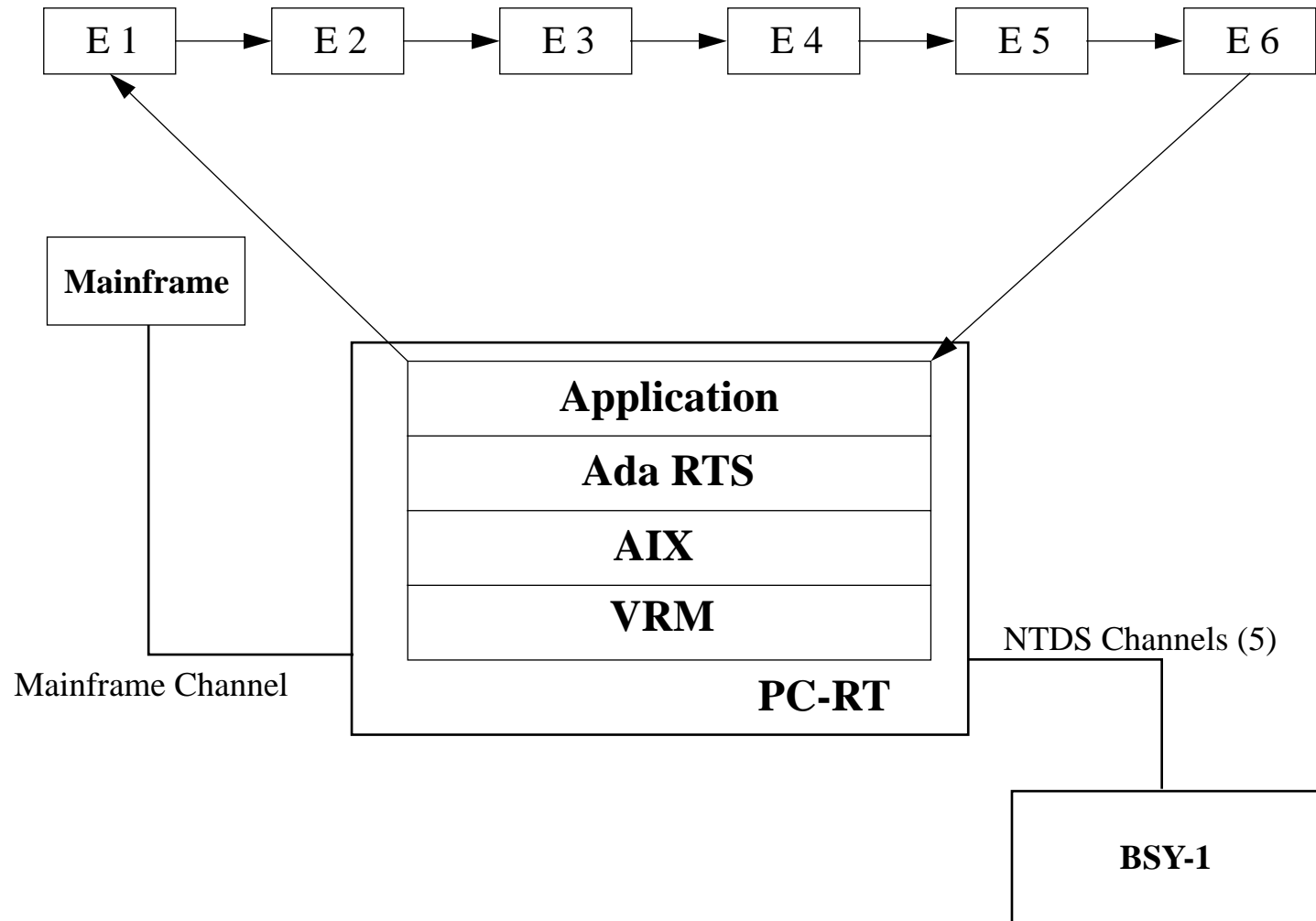


# System Configuration



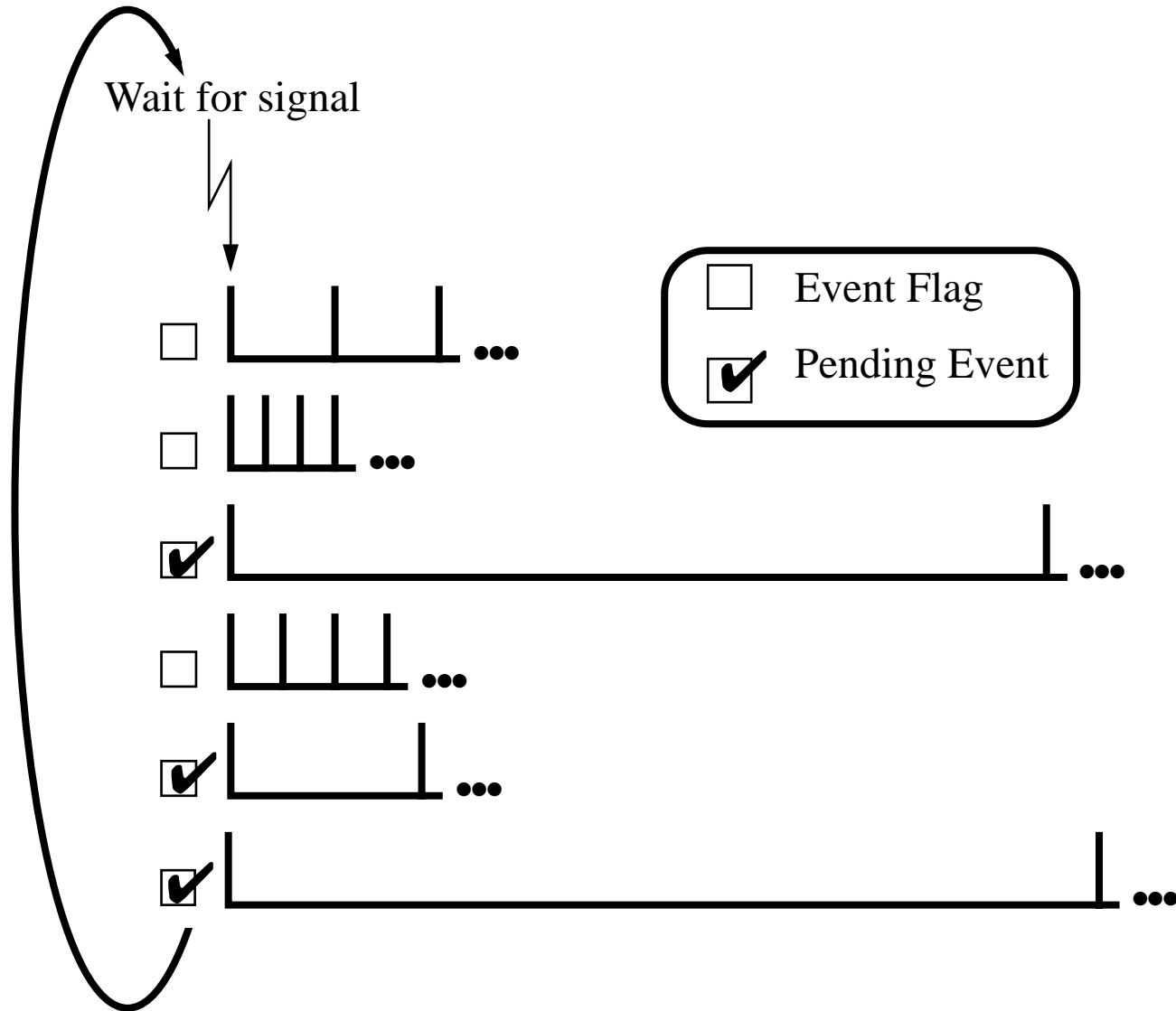


# Software Design



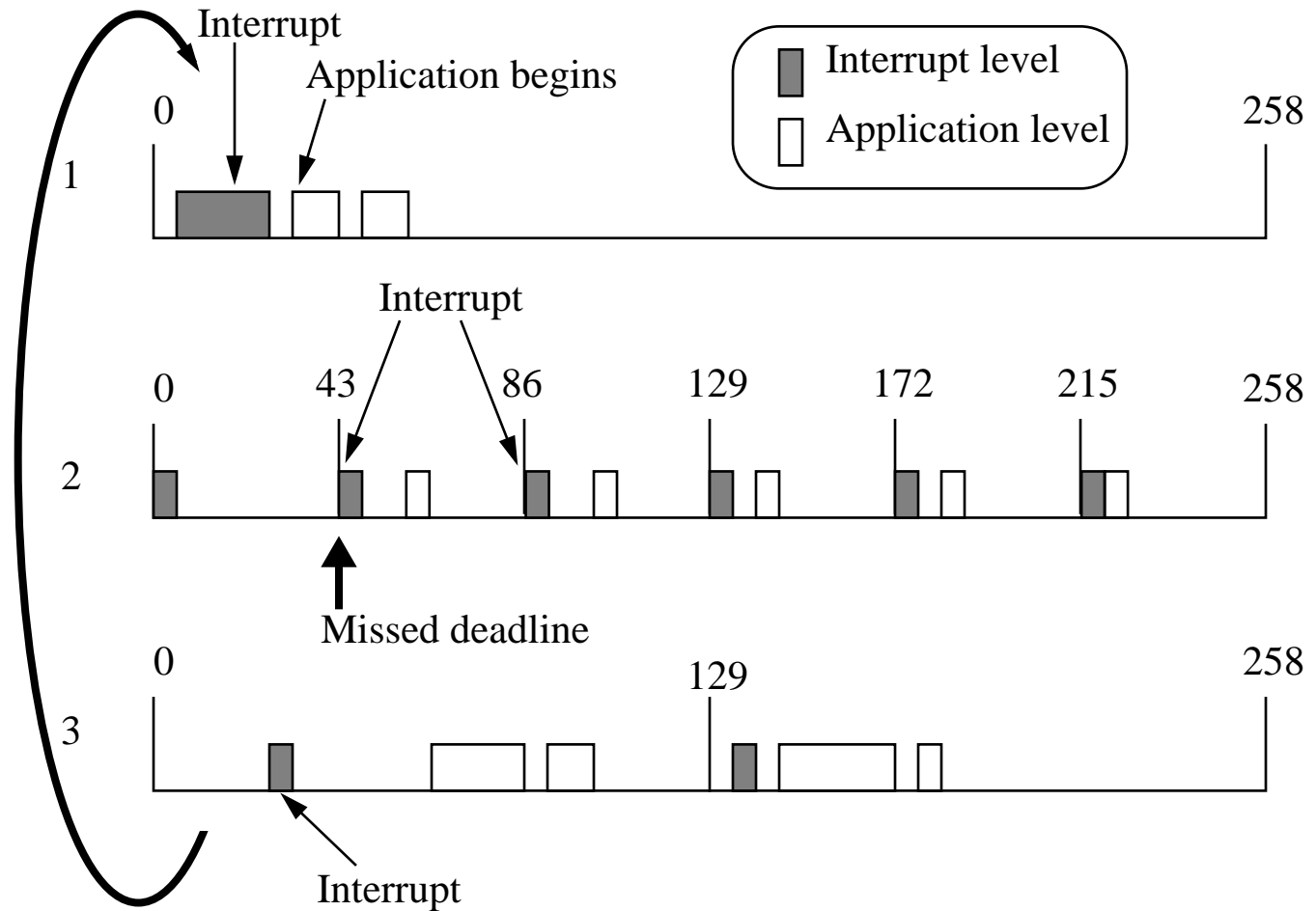


# Scheduling Discipline





# Execution Sequence: Original Design





# Problem Analysis by Development Team

**During integration testing, the PC-RT could not keep up with the mainframe computer.**

**The problem was perceived to be inadequate throughput in the PC-RT.**

**Actions planned to solve the problem:**

- **move processing out of the application and into VRM interrupt handlers**
- **improve the efficiency of AIX signals**
- **eliminate the use of Ada in favor of C**



# Data from Rate Monotonic Investigation

	$C_i$ (msec)	$C_a$ (msec)	$C$ (msec)	$T$ (msec)	$U$
Event 1	2.0	0.5	2.5	43	0.059
Event 2	7.4	8.5	15.9	74	0.215
Event 3	6.0	0.6	6.6	129	0.052
Event 4	21.5	26.7	48.2	258	0.187
Event 5	5.7	23.4	29.1	1032	0.029
Event 6	2.8	1.0	3.8	4128	0.001
Total					0.543

**Observe that total utilization is only 54%; the problem cannot be insufficient throughput.**





# Analyzing Original Design

Event ID	Arrival Period	Execution Time	Priority	Blocking Delays	Deadline
e1i	43	2.0	HW	0	n/a
e2i	74	7.4	HW	0	n/a
e3i	129	6.0	HW	0	n/a
e4i	258	21.5	HW	0	n/a
e5i	1032	5.7	HW	0	n/a
e6i	4128	2.8	HW	0	n/a
e1a	43	0.5	SW	0	43
e2a	74	8.5	SW	0	74
e3a	129	0.6	SW	0	129
e4a	258	26.7	SW	0	258
e5a	1032	23.4	SW	0	1032
e6a	4128	1.0	SW	0	4128



# Schedulability Model: Original Design

$$\mathbf{e1a} \quad \frac{C_{1a}}{T_{1a}} + \left[ \frac{C_{1i} + C_{2i} + C_{2a} + C_{3i} + C_{3a} + C_{4i} + C_{4a} + C_{5i} + C_{5a} + C_{6i} + C_{6a}}{T_1} \right] \leq U(1)$$

$$\mathbf{e2a} \quad \left[ \frac{C_{1i} + C_{1a}}{T_1} \right] + \frac{C_{2a}}{T_2} + \left[ \frac{C_{2i} + C_{3i} + C_{3a} + C_{4i} + C_{4a} + C_{5i} + C_{5a} + C_{6i} + C_{6a}}{T_2} \right] \leq U(2)$$

$$\mathbf{e3a} \quad \left[ \frac{C_{1i} + C_{1a}}{T_1} + \frac{C_{2i} + C_{2a}}{T_2} \right] + \frac{C_{3a}}{T_3} + \left[ \frac{C_{3i} + C_{4i} + C_{4a} + C_{5i} + C_{5a} + C_{6i} + C_{6a}}{T_3} \right] \leq U(3)$$

$$\mathbf{e4a} \quad \left[ \frac{C_{1i} + C_{1a}}{T_1} + \frac{C_{2i} + C_{2a}}{T_2} + \frac{C_{3i} + C_{3a}}{T_3} \right] + \frac{C_{4a}}{T_4} + \left[ \frac{C_{4i} + C_{5i} + C_{5a} + C_{6i} + C_{6a}}{T_4} \right] \leq U(4)$$

$$\mathbf{e5a} \quad \left[ \frac{C_{1i} + C_{1a}}{T_1} + \frac{C_{2i} + C_{2a}}{T_2} + \frac{C_{3i} + C_{3a}}{T_3} + \frac{C_{4i} + C_{4a}}{T_4} \right] + \frac{C_{5a}}{T_5} + \left[ \frac{C_{5i} + C_{6i} + C_{6a}}{T_5} \right] \leq U(5)$$

$$\mathbf{e6a} \quad \left[ \frac{C_{1i} + C_{1a}}{T_1} + \frac{C_{2i} + C_{2a}}{T_2} + \frac{C_{3i} + C_{3a}}{T_3} + \frac{C_{4i} + C_{4a}}{T_4} + \frac{C_{5i} + C_{5a}}{T_5} \right] + \frac{C_6}{T_6} + \left[ \frac{C_{6i}}{T_6} \right] \leq U(6)$$



# Schedulability Test: Original Design

$$\mathbf{e1a} \quad \frac{0.5}{43} + \left[ \frac{2.0 + 7.4 + 8.5 + 6.0 + 0.6 + 21.5 + 26.7 + 5.7 + 23.4 + 2.8 + 1.0}{43} \right] \leq U(1)$$

$$\mathbf{e2a} \quad \left[ \frac{2.0 + 0.5}{43} \right] + \frac{8.5}{74} + \left[ \frac{7.4 + 6.0 + 0.6 + 21.5 + 26.7 + 5.7 + 23.4 + 2.8 + 1.0}{74} \right] \leq U(2)$$

$$\mathbf{e3a} \quad \left[ \frac{2.0 + 0.5}{43} + \frac{7.4 + 8.5}{74} \right] + \frac{0.6}{129} + \left[ \frac{6.0 + 21.5 + 26.7 + 5.7 + 23.4 + 2.8 + 1.0}{129} \right] \leq U(3)$$

$$\mathbf{e4a} \quad \left[ \frac{2.0 + 0.5}{43} + \frac{7.4 + 8.5}{74} + \frac{6.0 + 0.6}{129} \right] + \frac{26.7}{258} + \left[ \frac{21.5 + 5.7 + 23.4 + 2.8 + 1.0}{258} \right] \leq U(4)$$

$$\mathbf{e5a} \quad \left[ \frac{2.0 + 0.5}{43} + \frac{7.4 + 8.5}{74} + \frac{6.0 + 0.6}{129} + \frac{21.5 + 26.7}{258} \right] + \frac{23.4}{1032} + \left[ \frac{5.7 + 2.8 + 1.0}{1032} \right] \leq U(5)$$

$$\mathbf{e6a} \quad \left[ \frac{2.0 + 0.5}{43} + \frac{7.4 + 8.5}{74} + \frac{6.0 + 0.6}{129} + \frac{21.5 + 26.7}{258} + \frac{5.7 + 23.4}{1032} \right] + \frac{1.0}{4128} + \left[ \frac{2.8}{4128} \right] \leq U(6)$$



# Utilization: Original Design

Event	Period (msec)	Preempt { $H_n$ }	Execute	Preempt { $H_1$ }	Total ( $f_i$ )
1a	43	0.000	0.012	2.456	2.468
2a	74	0.059	0.115	1.286	1.460
3a	129	0.274	0.005	0.676	0.955
4a	258	0.326	0.104	0.211	0.641
5a	1032	0.513	0.023	0.010	0.546
6a	4128	0.542	0.001	0.001	0.544

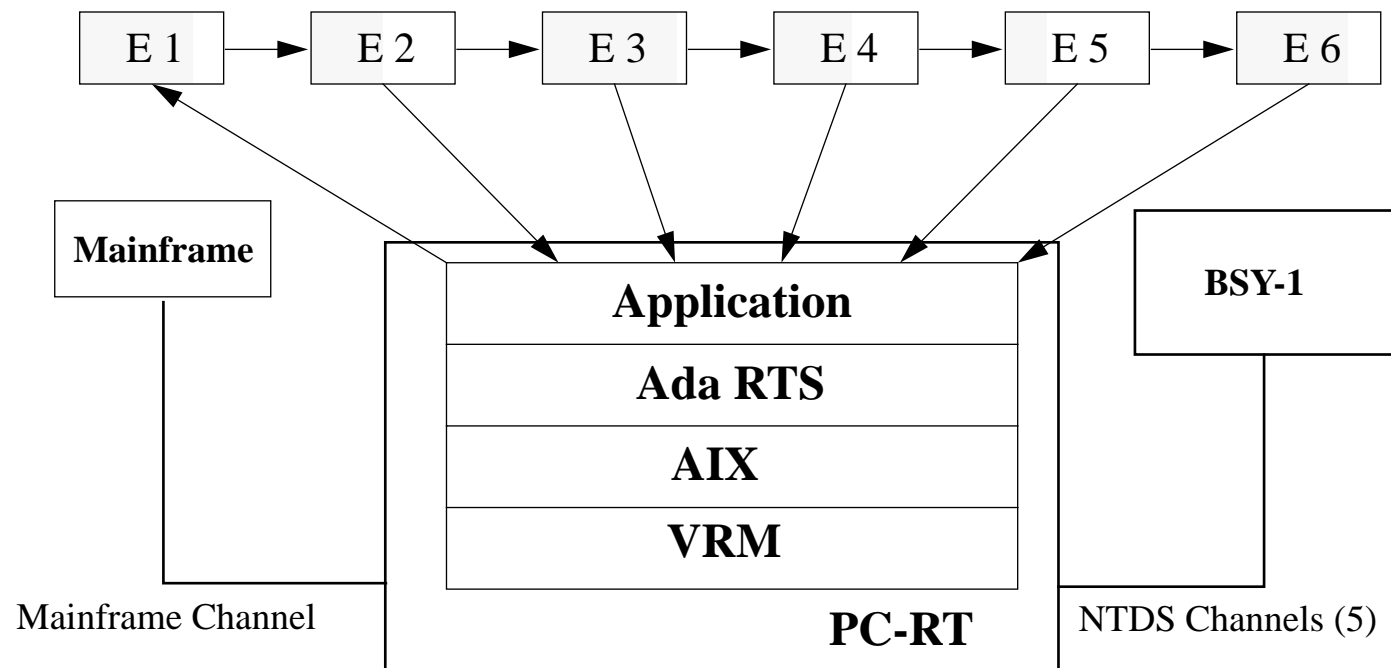
Effective utilizations ( $f_i$ ) for events 4, 5, and 6 are all under 69%. These events are schedulable.

The problem for events 1, 2, and 3 is excessive  $H_1$  preemption.



# Process Events in RM Order

<i>U</i>	5.9%	21.5%	5.2%	18.7%	2.9%	0.1%
<i>C<sub>i</sub></i>	2.0	7.4	6.0	21.5	5.7	2.8
<i>C<sub>a</sub></i>	0.5	8.5	0.6	26.7	23.4	1.0
<i>T</i>	43	74	129	258	1032	4128





# Schedulability Model: Process Events in RM Order

$$\mathbf{e1a} \quad \frac{C_{1a}}{T_1} + \left[ \frac{\max(C_{2a}, C_{3a}, C_{4a}, C_{5a}, C_{6a}) + C_{1i} + C_{2i} + C_{3i} + C_{4i} + C_{5i} + C_{6i}}{T_1} \right]$$

$$\mathbf{e2a} \quad \left[ \frac{C_{1i} + C_{1a}}{T_1} \right] + \frac{C_{2a}}{T_2} + \left[ \frac{\max(C_{3a}, C_{4a}, C_{5a}, C_{6a}) + C_{2i} + C_{3i} + C_{4i} + C_{5i} + C_{6i}}{T_2} \right]$$

$$\mathbf{e3a} \quad \left[ \frac{C_{1i} + C_{1a}}{T_1} + \frac{C_{2i} + C_{2a}}{T_2} \right] + \frac{C_{3a}}{T_3} + \left[ \frac{\max(C_{4a}, C_{5a}, C_{6a}) + C_{3i} + C_{4i} + C_{5i} + C_{6i}}{T_3} \right]$$

$$\mathbf{e4a} \quad \left[ \frac{C_{1i} + C_{1a}}{T_1} + \frac{C_{2i} + C_{2a}}{T_2} + \frac{C_{3i} + C_{3a}}{T_3} \right] + \frac{C_{4a}}{T_4} + \left[ \frac{\max(C_{5a}, C_{6a}) + C_{4i} + C_{5i} + C_{6i}}{T_4} \right]$$

$$\mathbf{e5a} \quad \left[ \frac{C_{1i} + C_{1a}}{T_1} + \frac{C_{2i} + C_{2a}}{T_2} + \frac{C_{3i} + C_{3a}}{T_3} + \frac{C_{4i} + C_{4a}}{T_4} \right] + \frac{C_{5a}}{T_5} + \left[ \frac{C_{6a} + C_{5i} + C_{6i}}{T_5} \right]$$

$$\mathbf{e6a} \quad \left[ \frac{C_{1i} + C_{1a}}{T_1} + \frac{C_{2i} + C_{2a}}{T_2} + \frac{C_{3i} + C_{3a}}{T_3} + \frac{C_{4i} + C_{4a}}{T_4} + \frac{C_{5i} + C_{5a}}{T_5} \right] + \frac{C_{6a}}{T_6} + \frac{C_{6i}}{T_6}$$



# Schedulability Test: Process Events in RM Order

$$\mathbf{e1a} \quad \frac{0.5}{43} + \left[ \frac{(26.7) + 2.0 + 7.4 + 6.0 + 21.5 + 5.7 + 2.8}{43} \right]$$

$$\mathbf{e2a} \quad \left[ \frac{2.5}{43} \right] + \frac{8.5}{74} + \left[ \frac{(26.7) + 7.4 + 6.0 + 21.5 + 5.7 + 2.8}{74} \right]$$

$$\mathbf{e3a} \quad \left[ \frac{2.5}{43} + \frac{15.9}{74} \right] + \frac{0.6}{129} + \left[ \frac{(26.7) + 6.0 + 21.5 + 5.7 + 2.8}{129} \right]$$

$$\mathbf{e4a} \quad \left[ \frac{2.5}{43} + \frac{15.9}{74} + \frac{6.6}{129} \right] + \frac{26.7}{258} + \left[ \frac{(23.4) + 21.5 + 5.7 + 2.8}{258} \right]$$

$$\mathbf{e5a} \quad \left[ \frac{2.5}{43} + \frac{15.9}{74} + \frac{6.6}{129} + \frac{48.2}{258} \right] + \frac{23.4}{1032} + \left[ \frac{1.0 + 5.7 + 2.8}{1032} \right]$$

$$\mathbf{e6a} \quad \left[ \frac{2.5}{43} + \frac{15.9}{74} + \frac{6.6}{129} + \frac{48.2}{258} + \frac{29.1}{1032} \right] + \frac{1.0}{4128} + \left[ \frac{2.8}{4128} \right]$$



# Utilization: Process Events in RM Order

Event	Period (msec)	Preempt $\{H_n\}$	Execute	Preempt $\{H_1\}$	Total $(f_i)$	Previous Total
1a	43	0.000	0.012	1.677	1.689	2.468
2a	74	0.059	0.115	0.948	1.122	1.460
3a	129	0.274	0.005	0.487	0.766	0.955
4a	258	0.326	0.104	0.207	0.637	0.641
5a	1032	0.513	0.023	0.010	0.546	0.546
6a	4128	0.542	0.001	0.001	0.544	0.544



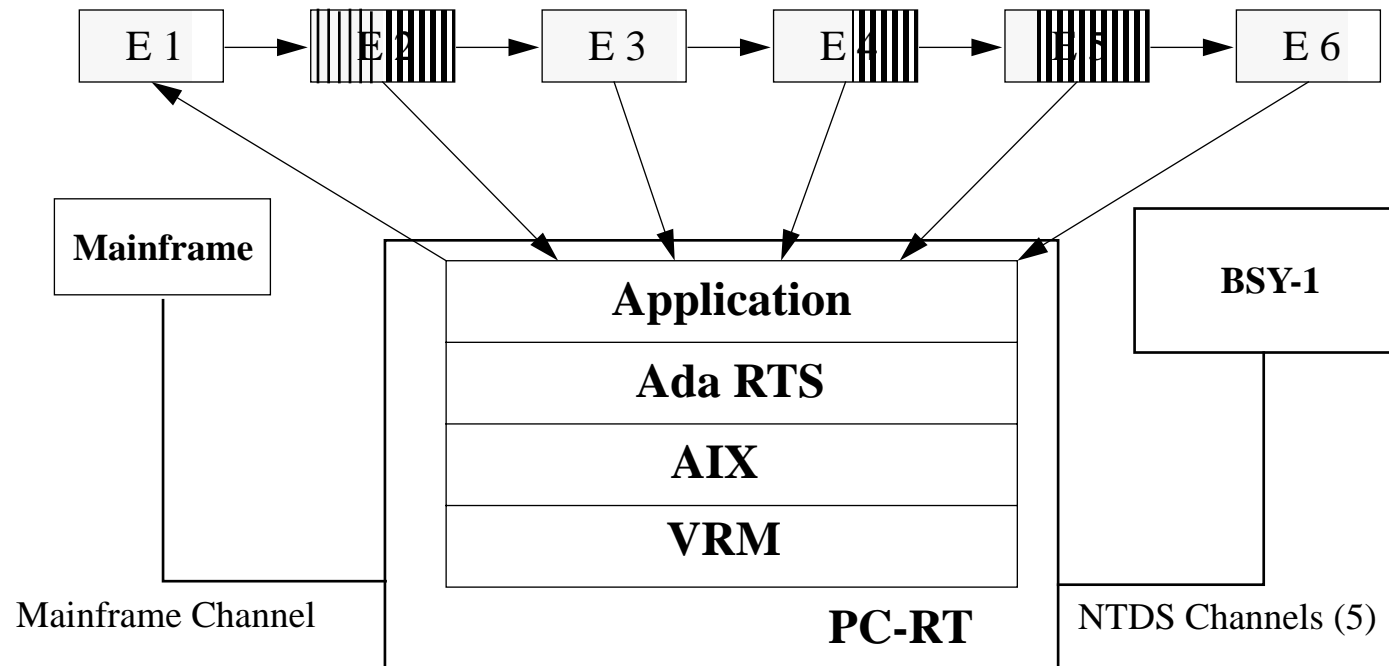


# Increasing Preemptibility

## Preemptible I/O

## Packetized Data Movement

$U$	5.9%	21.5%	5.2%	18.7%	2.9%	0.1%
$C_i$	2.0	7.4 (1.5)	6.0	21.5	5.7	2.8
$C_a$	0.5	8.5 (1.7)	0.6	26.7 (4.5)	23.4 (3.9)	1.0
$T$	43	74	129	258	1032	4128





# Schedulability Test: Preemptible I/O and Packetized Data Movement

$$\mathbf{e1a} \quad \frac{0.5}{43} + \left[ \frac{(4.5) + 2.0 + 1.5 + \mathbf{6.0} + \mathbf{21.5} + \mathbf{5.7} + \mathbf{2.8}}{43} \right]$$

$$\mathbf{e2a} \quad \left[ \frac{\mathbf{2.5}}{43} \right] + \frac{8.5}{74} + \left[ \frac{(4.5) + 7.4 + \mathbf{6.0} + \mathbf{21.5} + \mathbf{5.7} + \mathbf{2.8}}{74} \right]$$

$$\mathbf{e3a} \quad \left[ \frac{\mathbf{2.5}}{43} + \frac{\mathbf{15.9}}{74} \right] + \frac{0.6}{129} + \left[ \frac{(4.5) + 6.0 + \mathbf{21.5} + \mathbf{5.7} + \mathbf{2.8}}{129} \right]$$

$$\mathbf{e4a} \quad \left[ \frac{\mathbf{2.5}}{43} + \frac{\mathbf{15.9}}{74} + \frac{\mathbf{6.6}}{129} \right] + \frac{26.7}{258} + \left[ \frac{(3.9) + 21.5 + \mathbf{5.7} + \mathbf{2.8}}{258} \right]$$

$$\mathbf{e5a} \quad \left[ \frac{\mathbf{2.5}}{43} + \frac{\mathbf{15.9}}{74} + \frac{\mathbf{6.6}}{129} + \frac{\mathbf{48.2}}{258} \right] + \frac{23.4}{1032} + \left[ \frac{1.0 + 5.7 + 2.8}{1032} \right]$$

$$\mathbf{e6a} \quad \left[ \frac{\mathbf{2.5}}{43} + \frac{\mathbf{15.9}}{74} + \frac{\mathbf{6.6}}{129} + \frac{\mathbf{48.2}}{258} + \frac{\mathbf{29.1}}{1032} \right] + \frac{1.0}{4128} + \left[ \frac{\mathbf{2.8}}{4128} \right]$$



# Utilization: Preemptible I/O and Packetized Data Movement

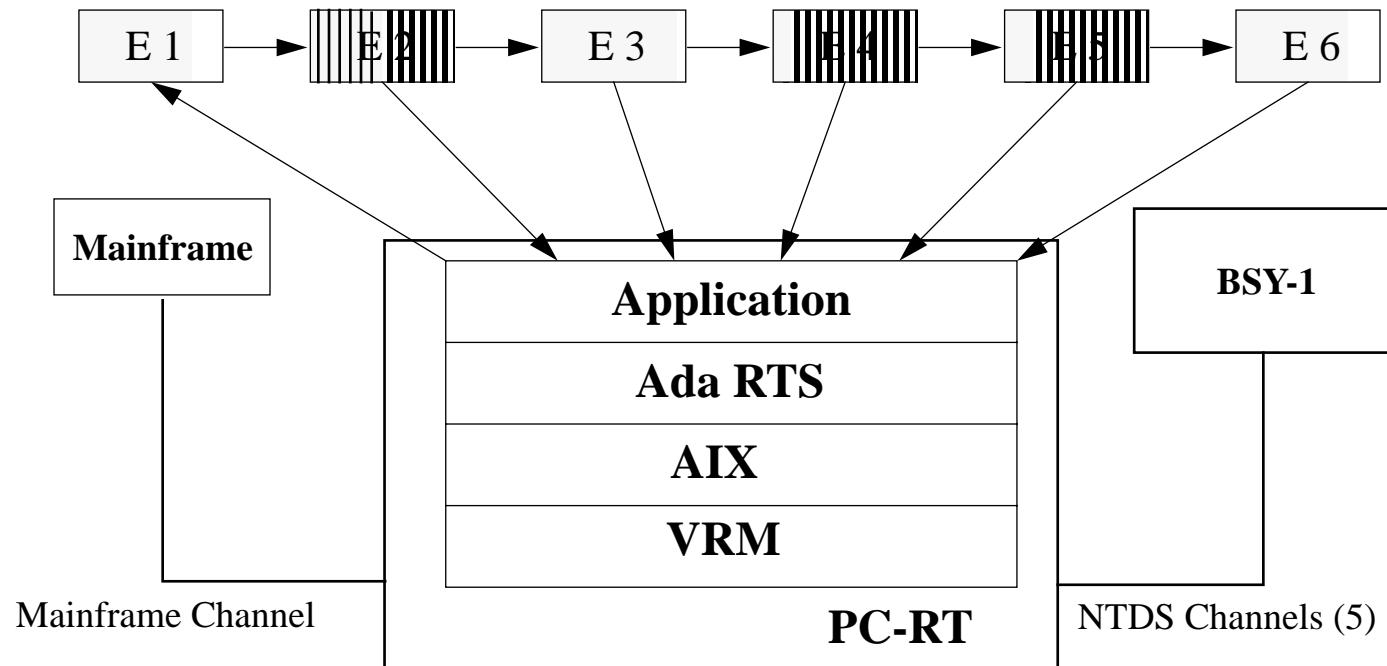
Event	Period (msec)	Preempt $\{H_n\}$	Execute	Preempt $\{H_1\}$	Total $(f_i)$	Previous Total
1a	43	0.000	0.012	1.024	1.036	1.689
2a	74	0.059	0.115	0.648	0.822	1.122
3a	129	0.274	0.005	0.314	0.593	0.766
4a	258	0.326	0.104	0.132	0.562	0.637
5a	1032	0.513	0.023	0.010	0.546	0.546
6a	4128	0.542	0.001	0.001	0.544	0.544

**According to the utilization bound test, all events now are schedulable, except event 1.**



# Streamlined Interrupt Handler

<i>U</i>	5.9%	21.5%		5.2%	18.7%	2.9%	0.1%
<i>C<sub>i</sub></i>	2.0	7.4 (1.5)		6.0	6.5	5.7	2.8
<i>C<sub>a</sub></i>	0.5	8.5 (1.7)		0.6	41.7 (4.5)	23.4 (3.9)	1.0
<i>T</i>	43	74		129	258	1032	4128





# Schedulability Test: Streamlined Interrupt Handler

$$\mathbf{e1a} \quad \frac{0.5}{43} + \left[ \frac{(4.5) + 2.0 + 1.5 + \mathbf{6.0} + 6.5 + \mathbf{5.7} + \mathbf{2.8}}{43} \right]$$

$$\mathbf{e2a} \quad \left[ \frac{2.5}{43} \right] + \frac{8.5}{74} + \left[ \frac{(4.5) + 7.4 + \mathbf{6.0} + 6.5 + \mathbf{5.7} + \mathbf{2.8}}{74} \right]$$

$$\mathbf{e3a} \quad \left[ \frac{2.5}{43} + \frac{15.9}{74} \right] + \frac{0.6}{129} + \left[ \frac{(4.5) + 6.0 + 6.5 + \mathbf{5.7} + \mathbf{2.8}}{129} \right]$$

$$\mathbf{e4a} \quad \left[ \frac{2.5}{43} + \frac{15.9}{74} + \frac{6.6}{129} \right] + \frac{41.7}{258} + \left[ \frac{(3.9) + 6.5 + \mathbf{5.7} + \mathbf{2.8}}{258} \right]$$

$$\mathbf{e5a} \quad \left[ \frac{2.5}{43} + \frac{15.9}{74} + \frac{6.6}{129} + \frac{48.2}{258} \right] + \frac{23.4}{1032} + \left[ \frac{1.0 + 5.7 + 2.8}{1032} \right]$$

$$\mathbf{e6a} \quad \left[ \frac{2.5}{43} + \frac{15.9}{74} + \frac{6.6}{129} + \frac{48.2}{258} + \frac{29.1}{1032} \right] + \frac{1.0}{4128} + \left[ \frac{2.8}{4128} \right]$$



# Utilization: Streamlined Interrupt Handler

Event	Period (msec)	Preempt $\{H_n\}$	Execute	Preempt $\{H_1\}$	Total $(f_i)$	Previous Total
1a	43	0.000	0.012	0.675	0.687	1.036
2a	74	0.059	0.115	0.445	0.619	0.822
3a	129	0.274	0.005	0.198	0.477	0.593
4a	258	0.326	0.162	0.074	0.562	0.562
5a	1032	0.513	0.023	0.010	0.546	0.546
6a	4128	0.542	0.001	0.001	0.544	0.544



# Summary: BSY-1 Trainer Case Study

## Recall original action plan:

- improve efficiency of AIX signals
- move processing from application to interrupts
- recode 17,000 lines of Ada to C

## Final actions:

- increase preemption and improve AIX
- move processing from interrupts to application
- modify 300 lines of Ada code
- RMA took 3 people 3 weeks